

SN. 10/055,722

ATTORNEY DOCKET NO. FUJI:203

Claim 1 calls for a first lateral MOS transistor having a smaller channel length than a second lateral MOS transistor. The examiner identifies Williams' 16V NMOS and 20V DMOS as corresponding to the claimed first and second MOS transistors, respectively. See Fig. 15A for example. The examiner then states that Williams's second MOS transistor (20V DMOS) has a smaller channel length than its first MOS transistor (16NMOS), without providing any explanation as to where Williams discloses such a feature. Note that the channel length refers to the length of the body region 122 in between the source region 152 and N-epi drain region. Applicant submits that in a VERTICAL DMOS transistor type (which is structurally different from a LATERAL MOS transistor type), the channel length is generally shorter, as compared to the length of the LATERAL MOS transistor type. See for example *MICROELECTRONIC CIRCUITS* by Sedra/Smith, Oxford University Press, 1998, pp. 792-795. Note that Williams' first and second MOS transistors are VERTICAL MOS transistor, whereas claim 1 calls for first and second LATERAL MOS transistors. Based on these distinctions, applicants submit that Williams could not have anticipated the pending claims.

Conclusion

Applicant submits that the pending claims patentably distinguish over the applied references and thus urge the examiner to issue an early Notice of Allowance. Should the examiner have any issues concerning this reply or any other outstanding issues remaining in this application, applicant urges the examiner to contact the undersigned to expedite prosecution.

Respectfully submitted,

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ATTACHMENT
MARKED UP VERSION

IN THE CLAIMS:

Claims 1 and 8 have been amended as follows:

--1. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first lateral MOS transistor and a second lateral MOS transistor integrated in the semiconductor substrate, wherein said second lateral MOS transistor has a lower threshold voltage than said first lateral MOS transistor and said first lateral MOS transistor has a smaller channel length than said second lateral MOS transistor; and

a punch-trough stopper area that surrounds a source area and a drain area of said first MOS transistor and provides a punch-through voltage resistance between said source area and said drain area.--

--8. (Amended) The semiconductor integrated circuit device according to Claim 1, wherein said source area includes a source LDD area and said drain area includes a drain side LDD area, and wherein the punch-through stopper area [had]has a pocket structure that enclose[d]s the source side LDD area and the drain side LDD area.--